

ABSTRACT

A method for controlling functional units in a processor is provided. During a configuration phase of the processor, a series of primary instruction words from the translation of a programme code are subjected to a division into series of instruction word bits. By this, the instruction words controlling the processor during a programme execution are generated with a full instruction word size and buffered in an instruction word memory (cache). The method improves the processor performance in the execution phase by increasing the degree of compression of the primary instruction words into divided instruction word bits. This is achieved independent of special features such as periodicity of the Function Instruction Word bit. First during the configuration phase, a division of a primary instruction word into a Tagged Very Long Instruction Word occurs. Next, this Tagged Very Long Instruction Word is transformed into a Headed Very Long Instruction Word, which includes a general header. The transformed Word has a code-compressed structure and replaces all functions of the Tagged Very Long Instruction Word.